

REMARKS

Appellant submits that the Decision of the Board, affirming the rejection of claims 1 and 5-8 under 35 U.S.C 102(b) as anticipated by Pilo (US 5,343,428), is based on faulty logic and an improper reading of the Appellant's own specification into the prior art, as will be explained below. Appellant therefore requests reconsideration of the decision and reversal of the rejection.

a) The Examiner and the Board erred in determining that Pilo teaches a reference node that serves as a reference voltage of a sense amplifier as claimed.

The Board adopted the Examiner's findings of facts and conclusions as set out in the Answer and adopted them as their own. For example, the Board states on page 7 of the Decision, "Furthermore, the Examiner states that in the absence of special definition of the term 'reference node,' the terms are interpreted under the broadest reasonable interpretation to simply mean a node having a voltage used as a point of reference (i.e., a comparison voltage)." Appellant agrees with the definition of a reference node as "a node having a voltage that is used as a point of reference." However, Appellant vehemently disagrees with a definition defining a reference node as "a node holding a comparison voltage." Such a definition would seem to imply that, in a single-ended sense amplifier, both the input data voltage and the reference voltage can be properly referred to as reference voltages, because they are compared to each other. This position is untenable.

Using the Examiner's (and the Board's) definition of a reference node as "a node having a voltage that is used as a reference," nodes 101 and 102 of Pilo clearly fail to meet this definition. Nodes 101 and 102 are not used as a reference point for anything. They simply hold the differential input data signals MUXLAT and MUXLAT*. Furthermore, even if the inaccurate definition, "a node holding a comparison voltage," is used, nodes 101 and 102 still fail to meet this definition. The voltages of nodes 101 and 102 are not compared to each other or to anything else. The operation of a differential sense amplifier is described in easily understandable terms in Pilo at column 1, lines 31-48. As can be seen there, it does not involve the comparison of the differential inputs. Furthermore, nowhere in the description of Figure 1 of Pilo does it describe the voltages of nodes 101 or 102 being compared to anything.

The Examiner and the Board also attach great weight to the fact that transistors 1025 and 1026 of Figure 10 of the present application add capacitance to node 1021 (the reference node) (finding of Fact 1), and to the fact that transistors 56 and 57 of Figure 1 of Pilo add capacitance to nodes 101 and 102 of Pilo (Finding of Fact 3). However, whether or not a node is “capacitive” has absolutely nothing to do with whether or not it is a reference node. That is, just because the reference node 1021 of the present invention is “capacitive” does not mean that all nodes that are capacitive are reference nodes.

The Examiner and the Board also attach great weight to the fact that claim 1 recites that the reference node is operable to store a reference signal corresponding to the input signal (Finding of Fact 2). However, the fact that the reference node of the present invention is operable to store a reference signal that corresponds to a signal that exists at the input of the amplifier prior to measurement of the data signal, does not mean that any node that stores an input data signal (such as nodes 101 and 102 of Pilo) is then a reference node. To hold otherwise is to improperly read the subject matter of the instant invention into the prior art.

On page 8 of the decision, the Board, using a broadest reasonable interpretation of the term “reference node” as “a node having a voltage that is used as a point of reference,” concludes that nodes 101 and 102 of Pilo can be reasonably interpreted to have a voltage that is used as a point of reference. Appellant submits that this is wrong. Nodes 101 and 102 of Pilo *cannot* be reasonably interpreted as having a voltage that is used as a point of reference. Under the broadest interpretation, nodes such as nodes 101 and 102, which merely store an input data signal, cannot be considered reference nodes. No one of skill in the art would call nodes 101 and 102 reference nodes.

Appellant further takes issue with the Examiner’s characterization (adopted by the Board) of the reference node 1021 of Figure 10 of the Appellant’s specification as “simply a capacitive node having a data signal applied thereto.” This characterization is inaccurate. Node 1021 is a reference node, which one of ordinary skill in the art would understand to mean it serves as a point of reference to compare with an input signal. As described in the specification, according to the present invention, at a point in time just prior to measurement of the input data signal, the input node 1004 is sampled and that value is used as the reference voltage during the subsequent measurement of the input data signal. The fact that the novel arrangement of the present

invention involves sampling the input node just prior to the measurement of the input data signal should in no way lead to the conclusion that all nodes (such as nodes 101 and 102 of Pilo) that hold an input signal are reference nodes.

For these reasons, Appellant submits that the Examiner and the Board erred in determining that Pilo teaches a reference node that serves as a reference voltage of a sense amplifier as claimed.

b) The Examiner and the Board erred in determining that Pilo teaches a timing circuit activating the sampling circuit a predetermined interval before measurement of the input signal is initiated as claimed.

The Board again adopted the Examiner's findings of facts and conclusions as set out in the Answer and adopted them as their own, without providing further explanation of why it chose to do so. Appellant submits that Pilo fails to teach "activating the sampling circuit a predetermined interval before measurement of the input signal *is initiated*," per claim 1. As set forth in the Appeal Brief, Appellant submits that it is precisely the CLK signal of Pilo that initiates the measurement of the input signal. Therefore, activating the sampling circuit and initiating the measurement of the input signal are one and the same, and therefore the CLK signal of Pilo cannot activate the sampling circuit a predetermined time before measurement of the input signal is initiated, as argued in the Appeal Brief.

Thus, Appellant disagrees with the Boards's finding that Pilo teaches the activation of the sampling circuit a predetermined interval before the measurement of the input signal is *initiated*. In reaching this conclusion, the Board construes the activation of the sampling circuit per claim 1 to occur upon the application of the CLK signal to the inverter 36 and to the transfer gate 40 of Pilo. The board further construes the initiation of the measurement of the input signal per claim 1 to occur at transistors 26 and 27 of Pilo (page 10, 2nd paragraph, of the Decision). This reading is counter to the plain wording of claim 1. Claim 1 sets forth "a timing circuit activating the sampling circuit a predetermined interval before measurement of the input signal is initiated, the sampling circuit admitting the input signal to the reference node *thereby*." Therefore, per this wording, the activation of the sampling circuit admits the input signal to the reference node, all

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of which occurs before measurement of the input signal. But the Examiner and the Board deem nodes 101 and 102 of Pilo to be the “reference nodes” per claim 1. Nodes 101 and 102 comprise the inputs to transistors 26 and 27. Therefore the admission of the input signal to the “reference nodes” 101, 102 *cannot* occur *before* measurement of the input signal is initiated at transistors 26 and 27.

For these reasons, Appellant submits that the Examiner and the Board erred in determining that Pilo teaches a timing circuit activating the sampling circuit a predetermined interval before measurement of the input signal is initiated as claimed.

c) Conclusion

In view of the foregoing, Appellant requests rehearing of the Appeal, reversal of the rejection of claims 1 and 5-8 depending therefrom, and allowance of said claims.

The Commissioner is hereby authorized to charge additional fee(s) or credit overpayment(s) to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

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Respectfully submitted,

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